IN THE CLAIMS:

Please cancel claim 15 and amend claims 16-20 as follows:

Claim 1. (original) A combinational circuit comprising:

a plurality of multipliers, independently performing two or more multiplications for coded digital signals in a Galois extension field $GF(2^m)$, where m is an integer equal to or greater than 2,

wherein said multipliers include

an input side XOR calculator,

an AND calculator, and

an output side XOR calculator, and wherein said multipliers share said input side XOR calculator.

Claim 2. (original) The combinational circuit according to claim 1, wherein the input of said multipliers is commonly used.

Claim 3. (original) The combinational circuit according to claim 1, that is used for:

an error location calculator that calculates an error location for a digital signal transmitted using wavelength division multiplexing, and

for an error value calculator.

Claim 4. (original) The combinational circuit according to claim 1, wherein syndromes obtained by said coded digital signal are input.

Claim 5. (original) The combinational circuit according to claim 1, that is used for at least one of decoding, error correction and encryption.

Claim 6. (original) The combinational circuit according to claim 1, that is used for a coding circuit and a decoding circuit for cryptography.

Claim 7. (original) A combinational circuit for performing a logical sum calculation for a Galois extension field $GF(2^m)$, where m is an integer equal to or greater than 2, comprising:

a plurality of multipliers, each of which includes an adder connected between an AND calculator and an output side XOR calculator,

wherein said output side XOR calculator is used in common, and

wherein outputs of said AND calculators in said multipliers are added by said adders, and addition results are calculated by said output side XOR calculator that is used in common.

Claim 8. (original) The combinational circuit according to claim 7, wherein said multipliers have an input that is commonly used, and said input side XOR calculator is used in common by said multipliers.

Claim 9. (original) The combinational circuit according to claim 7, that is used for:

an error location calculator for calculating an error location for a digital signal transmitted using wavelength division multiplexing, and

an error value calculator.

Claim 10. (original) The combinational circuit according to claim 7, wherein syndromes obtained by said coded digital signal are input.

Claim 11. (original) The combinational circuit according to claim 7, that is used for at least one of decoding, error correction and encryption.

Claim 12. (original) The combinational circuit according to claim 7 that is used for a coding circuit and a decoding circuit for cryptography.

Claim 13. (original) An encoder including the combinational circuit according to claim 1 or claim 7.

Claim 14. (original) A decoder including the combinational circuit according to claim 1 or claim 7.

Claim 15. (canceled)

Claim 16. (currently amended) A semiconductor device used for processing a digital signal, said device comprising:

input means, for receiving a coded digital signal;

processing means, for processing said coded digital signal and for calculating coefficients of error locator polynomial and coefficients of error value polynomial; and

output means, for outputting a digital signal obtained by correcting errors using said coefficients of error locator polynomial and said coefficients of error value polynomial,

wherein said input means is constituted by a sequential circuit, and said processing means is constituted by a combinational circuit, and

~~The semiconductor device according to claim 15,~~ wherein said combinational circuit includes:

a plurality of multipliers, independently performing two or more multiplications for coded digital signals in a Galois extension field $GF(2^m)$, where m is an integer equal to or greater than 2,

wherein said multipliers include

an input side XOR calculator,

an AND calculator, and

an output side XOR calculator, and

wherein said multipliers share said input side XOR calculator.

Claim 17. (currently amended) A semiconductor device used for processing a digital signal, said device comprising:

input means, for receiving a coded digital signal;

processing means, for processing said coded digital signal and for calculating coefficients of error locator polynomial and coefficients of error value polynomial; and

output means, for outputting a digital signal obtained by correcting errors using said coefficients of error locator polynomial and said coefficients of error value polynomial,

wherein said input means is constituted by a sequential circuit, and said processing means is constituted by a combinational circuit, and

~~The semiconductor device according to claim 15,~~ wherein said combinational circuit includes:

a logical sum calculator for a Galois extension field $GF(2^m)$, where m is an integer equal to or greater than 2,

wherein said multipliers include an adder connected between said AND calculator and said output side XOR calculator,

wherein said output side XOR calculator is used in common, and

wherein outputs of said AND calculators in said multipliers are added by said adders, and addition results are calculated by said output side XOR calculator that is used in common.

Claim 18. (currently amended) The semiconductor device according to claim ~~15~~ 16, wherein said multipliers have commonly used input, and said input side XOR calculator is used in common by said multipliers.

Claim 19. (currently amended) The semiconductor device according to claim ~~15~~ 16, wherein said combinational circuit is used for an error location calculator, for calculating an error location for a digital signal transmitted using wavelength division multiplexing, and for an error value calculator.

Claim 20. (currently amended) The semiconductor device according to claim ~~15~~ 16 that is used for at least one of decoding, error correction and encryption.